PROGRAMMING MANUAL FOR MODELS

7164/7164H,

7166/7166H, 7167/7167H,

7186/7186H, AND 7187/7187H

1. CAMAC DATAWAY OPERATIONS

1.1 Writing Data

F(16)•A(X): Write to data memory for channel (X+1).

1.2 Reading Data

F(0)•A(X): Read event data memory for Channel (X+1). Data word contains pedestal corrected data and the channel number. Data is present regardless of sparsification and is read non-destructively.

F(4)•A(0): Read Sparse Data. Only those channels with data that falls between the Upper and Lower Thresholds are read, starting with the highest numbered channel. Each read presents the next channel on the hit list. As each channel is read, its bit in the Hit Register is reset. Reading an empty buffer returns Q false, X true.

16 13	12 1
Channel #	Channel Data

Channel Data Format

1.3 Set the Control Register

F(19)•A(0)•D(X): Selectively enable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Enable the Pedestals
D2=1 Enable the Lower Thresholds
D3=1 Enable the Upper Thresholds
D4 to D15 = 1 No Action

1.4 Reset the Control Register

F(23)•A(0)•D(X): Selectively disable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Disable the Pedestals
D2=1 Disable the Lower Thresholds
D3=1 Disable the Upper Thresholds
D4 to D15 = 1 No Action

1.5 Read the Control Register

F(6)•A(0): Read the control register. This tells which of the Pedestal, Upper Threshold or Lower Threshold are enabled, as well as the programming of the Conversion Delay.

16 9	8 4	3	2	1
MSB Delay Time LSB	0	UT Enabled	LT Enabled	PED Enabled

Control Register Data Format

1.6 Read the Hit Register

F(6)•A(1): Read the Hit Register. Shows which channels' pedestal corrected data fall within their Upper and Lower Thresholds. A 1 in any position indicates the channel has passed sparsification. For example, 0100 0010 0000 1001 shows that data on channels 1, 4, 10, and 15 have passed sparsification. These are the channels which will be read using the sparse data read function (F4).

16	1
Channel 16	Channel 1

Hit Register Data Format

1.7 Read and Write the Parameter Memory

Signed two's complement arithmetic is used. Pedestals occupy 13 bits giving a range of -4096 ($1000) to +4095 ($0FFF). Thresholds are 12 bits, ranging from 0 to 4095.

1.7.1 Select the Parameter

F(17)•A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)•A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)•A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

1.7.2 Write the Data

F(20)•A(X): Write the Pedestal, Upper or Lower Threshold for Channel (X+1) as selected by the most recent F17 operation.

1.7.3 Read the Data

F(1)•A(X): Read the Parameter Memory pointed to by the most recent F17 operation for channel (X+1).

1.8 Test Functions

1.8.1 Run a Test from fhe Test Registers

1.8.1.1 Select a Pattern

1.8.1.1.1 Select the Test Registers

F(17)•A(4): Select the Test Register for the next F20 operation.

1.8.1.1.2 Select a Pattern

F(20)•A(X): Program the Test Register if it was selected by the most recent F17 operation.

X	Pattern
0	001001001001
1	010010010010
2	100100100100
3	111111111111

1.8.1.2 Run A Test

F(25)•A0: Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.

1.8.2 Run A Front End Full Scale Test

Models 7166/7166H, 7167/7167H, 7186/7186H and 7187/7187H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

Model 7164/7164H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/20 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 1/4 full scale applied to the front end.

1.9 LAM

LAM is set during digitization when pedestal corrected data for at least one channel falls between that channel's Upper and Lower Thresholds.

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(10): Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

1.10 Resets

F(9): Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(11)•A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)•A(1): Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)•A(2): Reset the Test Register. Occurs on S2 strobe.

F(11)•A(3): Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

2. CAMAC NON-DATAWAY COMMANDS

C, Z: Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I: Inhibits front end functions.

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